# Proton Test Results for SEU and MBU in Texas Instruments 65 nm CMOS SRAMs

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## I. Introduction

These experiments were undertaken to study the influence of proton energy and angle of incidence on Single Event Upset (SEU) and Multiple Bit Upset (MBU) in 65 nm CMOS SRAMs. The memories were fabricated by Texas Instruments (TI).

## II. SRAM Description

The SRAMs were bonded directly to test boards at Radiation Assured Devices in Colorado Springs, CO using a layout designed at GSFC. The identification information for these SRAMs according to TI is:

Test Chip: x1886

Lot # 4071614

Wafer # 7

Module: T21YR8M

The device technology is 65 nm bulk CMOS. There are 8 memory sections consisting of 1 Mbit each. Two sections are high performance (HP), which consist of the largest size transistors. The remaining 6 sections consist of smaller transistors for high density applications. There are two types of high density memory sections - two Mbits identified as HD-B and 4 Mbits identified as HD-POR.

## III. Test Facilities

**Facilities:** In order to cover the complete proton energy range of interest 3 facilities were used – the NASA/GSFC Van De Graaff accelerator, the University of California, Davis Cyclotron and the Indiana University Cyclotron. These facilities are denoted in the Table below as “GSFC”, “UCD” and “IU”, respectively.

**Proton Energies:** The following table shows the primary proton beam energies used at the different facilities, degraders used exterior to the beam line and proton energies incident on the device under test (DUT).

| Facility: | Primary Proton Energy: | Exterior Degrader: | Proton Energy at DUT: |
|---|---|---|---|
| GSFC | 0.8 | - | 0.8 |
| GSFC | 0.9 | - | 0.9 |
| GSFC | 1.0 | - | 1.0 |
| GSFC | 1.2 | - | 1.2 |
| GSFC | 1.4 | - | 1.4 |
| UCD | 14.6 | 9.2 mil Ta, 4 mil Al | 2.6 |
| UCD | 14.6 | 9.2 mil Ta, 3 mil Al | 3.1 |
| UCD | 14.6 | 9.2 mil Ta | 4.6 |
| UCD | 14.6 | 5 mil Ta, 4 mil Al | 8.1 |
| UCD | 67.5 | 632 mil Al | 10.7 |
| UCD | 14.6 | 1 mil Ta | 12.2 |
| UCD | 67.5 | 573 mil Al | 19.8 |
| UCD | 67.5 | 512 mil Al | 27.3 |
| UCD | 67.5 | 323.5 mil Al | 43.7 |
| UCD | 67.5 | - | 63.0 |
| IU | 100 | - | 97.8 |
| IU | 200 | - | 198 |

**Flux:** The fluxes used for testing were in the range of $10^6$ p/cm$^2$/s at UCD and IU and in the range of $10^4$ p/cm$^2$/s at GSFC.

**Fluence:** SEU/MBU tests were run to acquire sufficient statistics. In order to ensure that MBU were due to single protons the number of upset bits per irradiation was kept under 800. This is 4 orders of magnitude less than the total number of bits in the memory.

## IV. Test Conditions

**Test Temperature:** Room Temperature
**Operating Frequency:** Static
**Power Supply Voltage:** $V_{dd}$ = 1.2 V; n-well bias (VNWA) = 0.5 V to maximize the number of working bits

**Test Pattern:** Logical checkerboard

**Angular Data:** Data were taken at the GSFC facility using protons that were normally incident on the DUT. At the UC Davis and IU facilities data were taken using protons that were both normally incident and incident at a 78.5 degree angle to the DUT. From a macroscopic view the chip is laid out with alternating columns of n-wells and p-wells. For the 78.5 degree angle irradiations the test board was oriented such that the protons were incident (nearly) parallel to the n- and p-well columns. The test set-ups are shown in Figures 1 and 2.

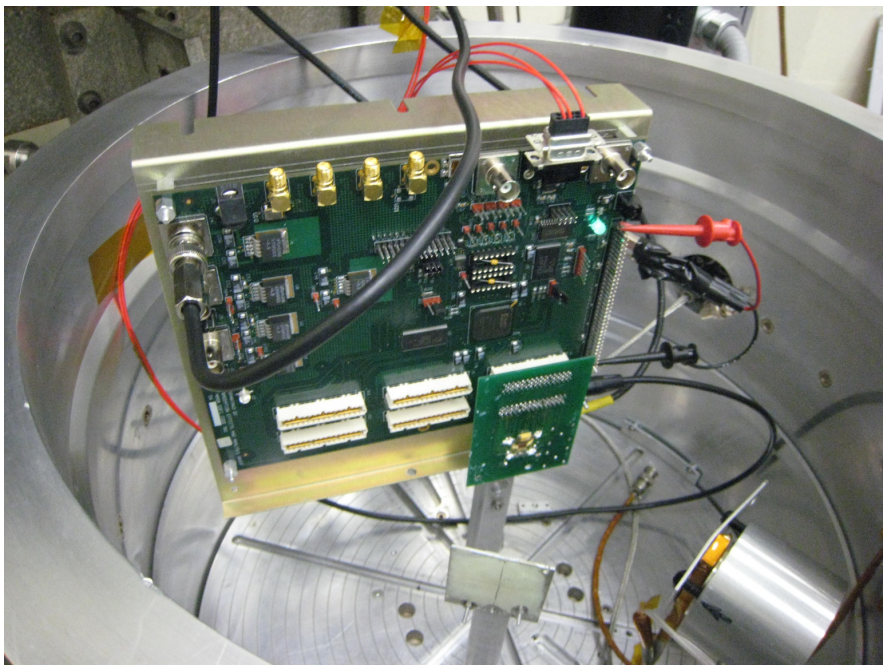

Figure 1. Test set-up at the NASA/GSFC Van De Graaff accelerator

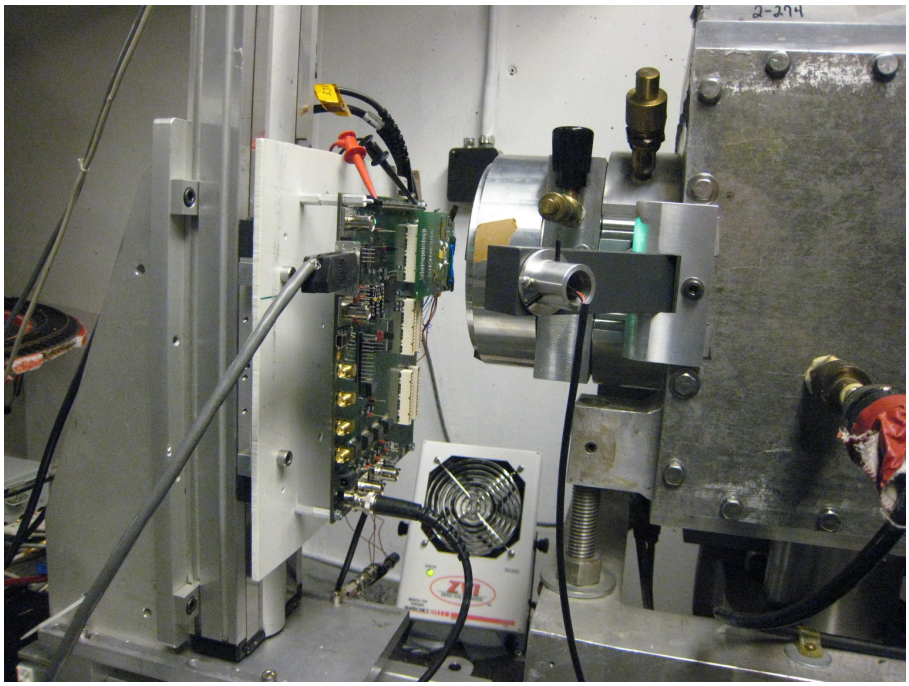

Figure 2. Test set-up used for the University of California, Davis Cyclotron and Indiana University Cyclotron Facilities (photo taken at UC Davis)

**Monitoring TID:** Supply (leakage) current $I_{dd}$ was measured after each irradiation to monitor parametric degradation from TID. No significant change was observed during testing.

# V. Results

*A. One-Bit Upset Cross Section Dependence on Proton Energy*

Figures 3 and 4 show the measured 1-bit upset cross sections as a function of incident proton energy at the DUT. Figure 3 is for normally incident protons and figure 4 is for 78.5 degree grazing incidence.

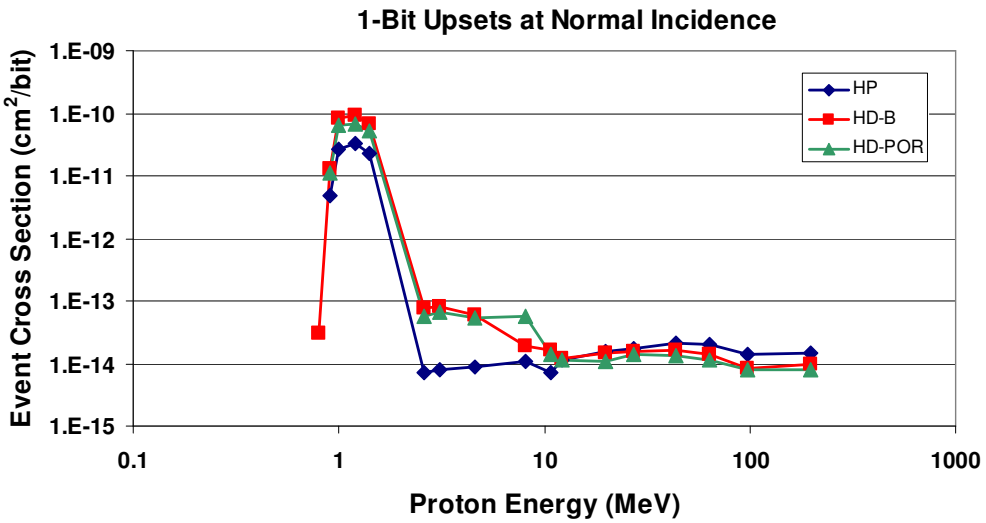


Figure 3. 1-bit upset cross sections for protons normally incident on TI 65 nm CMOS SRAMs

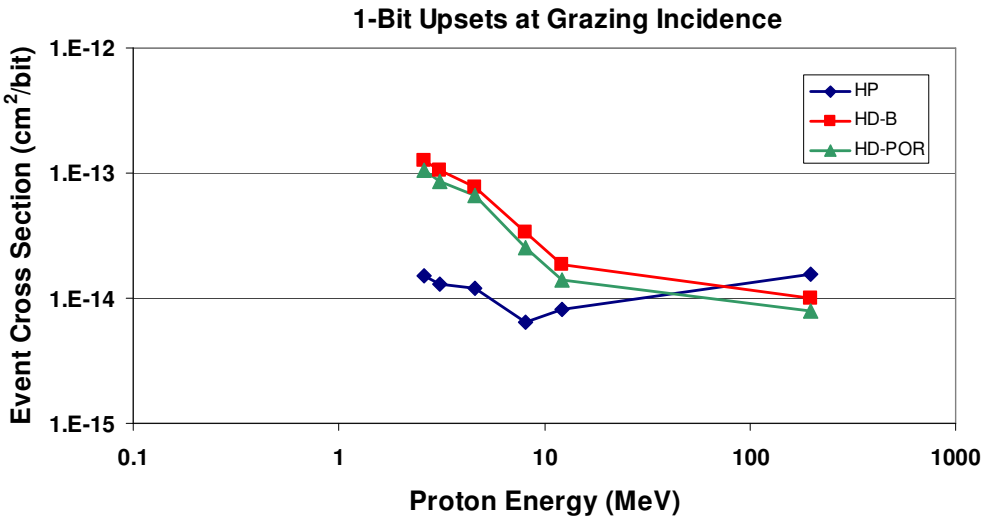


Figure 4. 1-bit upset cross sections for protons incident at a 78.5 degree grazing angle (nearly) parallel to the n- and p-well columns of TI 65 nm CMOS SRAMs

*B. MBU Cross Section Dependence on Proton Energy*

Figures 5 and 6 show the measured MBU cross sections as a function of incident proton energy at the DUT. Figure 5 is for normally incident protons and figure 6 is for 78.5 degree grazing incidence.

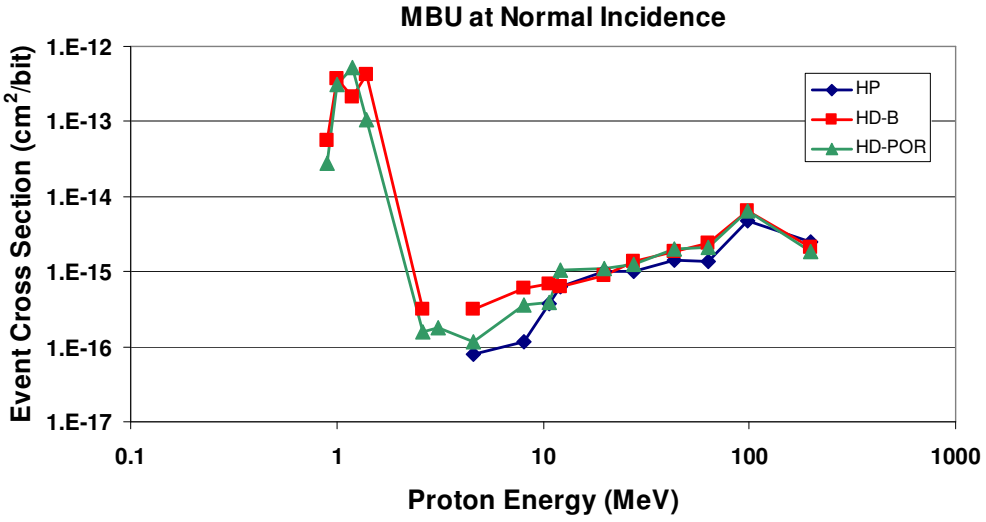


Figure 5. MBU cross sections for protons normally incident on TI 65 nm CMOS SRAMs

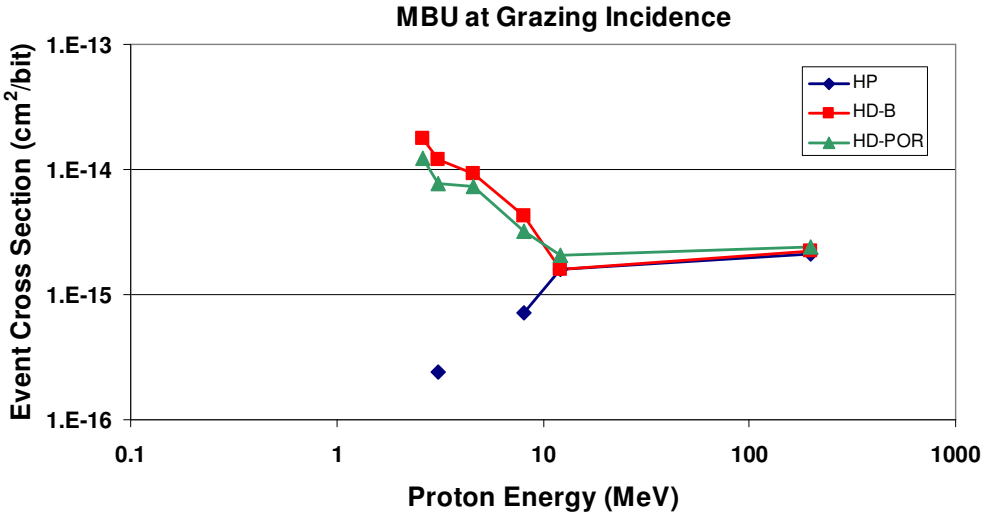


Figure 6. MBU cross sections for protons incident at a 78.5 degree grazing angle (nearly) parallel to the n- and p-well columns of TI 65 nm CMOS SRAMs

*C. Total Event Cross Section Dependence on Proton Energy*

Figures 7 and 8 show the measured total event cross sections as a function of incident proton energy at the DUT. Figure 7 is for normally incident protons and figure 8 is for 78.5 degree grazing incidence.

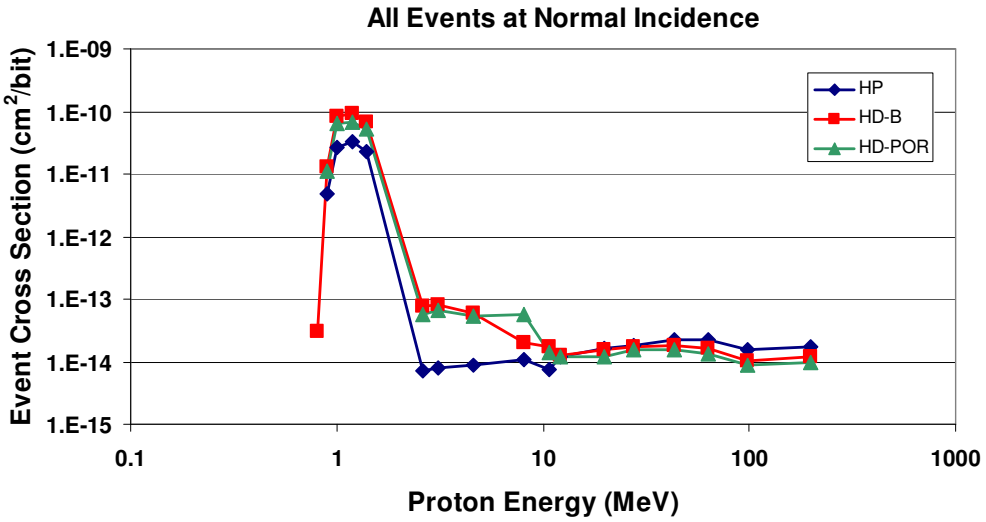


Figure 7. Total event cross sections for protons normally incident on TI 65 nm CMOS SRAMs

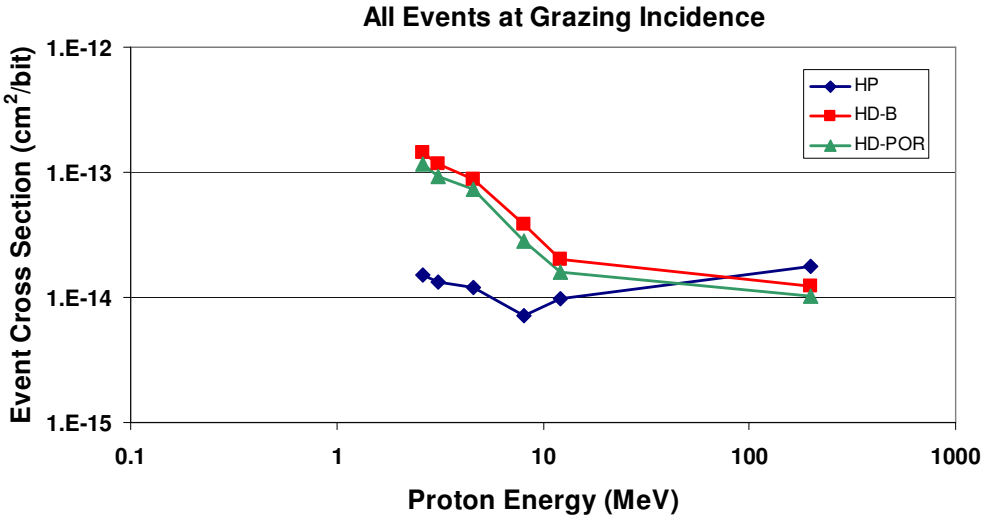


Figure 8. Total event cross sections for protons incident at a 78.5 degree grazing angle (nearly) parallel to the n- and p-well columns of TI 65 nm CMOS SRAMs

## VI. Summary

In this work we have measured the proton energy dependence of single and multiple bit upset cross sections in TI 65 nm CMOS SRAMs. These memories contained high performance cells and 2 types of high density cells. For normally incident ions, the cross sections peak sharply for all cell types at energies slightly more than 1 MeV. At these low energies data at grazing angles could not be taken. The high density cells generally showed larger cross sections for energies less than about 10 MeV. For energies greater than 10 MeV the cross sections for all cell types were similar.